LOW POWER PHASE FREQUENCY DETECTOR (PFD) FOR PHASE LOCKED LOOP (PLL) APPLICATION

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In Phase Locked Loop (PLL) system, Phase Frequency Detector(PFD) is a device which functioned to compares frequency and phaseof two input signals. The detector has two inputs which camefrom adividedVoltage Controlled Oscillator(VCO)output and external source. PFD hastwo outputs which instruct subsequent circuitry on how to adjust to lock onto the phase.Based on the current demanding of low power consumption in electronics devices, designing the PFD with low power has become main concerns and challenge to the circuitdesigner. Related to these issues, PFD design using forward body biased (FBB) technique has been proposed in this work. Then, the PFD with FBB performance is compared to the conventional PFD in term of power consumption. All the circuits have been designed and simulated using Mentor Graphic software in Silterra 0.13µm environment standard CMOS technology. By applying FBB in PFD circuit with supply voltage 0.8V and body voltage 0.4V, the circuit only consumed 9.1734nW power, compared to the conventional circuit power consumption 242.25nW. Basedon obtained result, it shows that the FBB PFD improves the power consumption with 96% reduction when compared to the conventional circuit.